**Mohit**

**6+ Years in Design Verification**

**Professional Experience**

2022 – Present **Pre-Silicon Validation Engineer**

Samsung SSIR, Bangalore (Client)

2016 – 2022 Sr. **Design Verification Engineer**

Client: Abilis Design Systems

**VLSI Domain Skills**

**Validation Domain Skills**

T32 Debugger, Coresight ARM,

Synopsys Zebu, Cadence Palladium

**Technical Skills**

Tools Used: Cadence NCSim, IMC, Simvision,

QuestaSim, Xilinx Vivado

FPGA: Zync Zedboard-ZC702

**Verification Domain Skills**

HDL/HVL: Verilog, System Verilog

Methodology: UVM

**Projects**

1. **Validation via T32 Debugger on Live Environment:**

Samsung Project (Present)

**Description:** Validation for various Attributes such as CTI, System Reset, SRAM/SFR Stress, SFR Access with Password, Debug Register Access via AHB-AP etc.

**Roles and Responsibility:**

Project Specification

CMM Script Handling

Debugging via Verdi

Backdoor Boot code Compilation

1. **Verification of TDM switch for Modem:**

**Description:** TDM switch is used to make use of the bandwidth of channels with maximum efficiency via shared interface pipes. It Supports E1 bit rate and time slots (32 time slots or 32 DSO channels at bit rate 2.048Mbps).

**Roles and Responsibility:**

Project Specification

Created Verification plan

Developed SV-UVM based verification plug & play env.

Created testcase sequences to verify various key features.

Worked on functional coverage model

Closed functional coverage as 100%

## Verification of Icemelter on IP & SOC level:

## Description: Icemelter is responsible to monitor the debugger probe activity on the IO pads and enable the debugger subsystem to connect to SoC.

**Roles and Responsibility:**

Understood the verification environment & the SOC test bench architecture.

Created SV based testcases to ensure the correct detection of pattern and enabling the debug control.

Analyzed toggle coverage.

1. **SRAM Controller Verification:**

**Description:** SRAM controller acts as an interface between the AHB system bus and the integrated system RAM. It converts the protocol between the system bus and the dedicated RAM array interface.

**Roles and Responsibility:**

Project Specification

Created Verification plan

Developed SV-UVM based verification

Created testcase to verify mem access and address decoding.

Closed toggle coverage as 100%

1. **Verification of UART slave:**

**Description:** UART is a hardware communication protocol that uses asynchronous serial communication with configurable speed. The device is interfaced in both master and slave mode and capable to read the sensor data to be interfaced with.

**Roles and Responsibility:**

Developed SV-UVM based verification plug & play env.

Created testcase sequences to verify various key features.

Create functional coverage model

Closed functional coverage as 100%

1. **Verification of DSPI:**

**Description:** SPI is a serial interfaced protocol used for communication in embedded systems. It’s a four-pin protocol. Device is supposed to communicate with external world for data transfer to-and-fro.

**Roles and Responsibility:**

Created Verification plan

Developed C, SV-UVM based verification plug & play envoi.

Created testcase sequences to verify various key features.

1. **Verification of AMBA Protocol-AHB Lite (Slave)**

AHB Lite (Slave) with Burst operation – In-house Project

**Description:** AHB is a protocol of AMBA bus which is intended to address the requirements of high-performance synthesizable designs. It is a high-performance system bus that supports multiple bus masters and provides high-bandwidth operation.

**Roles and Responsibilities:**

AMBA AHB protocol specification.

Created the Verification Plan.

Created Verification environment using UVM Methodology.

Worked on self-checking TB.

Sequence generated for Single Transfer, Increment and wrapping Burst transfers.

Worked on Pipelined Driver, Monitor, Scoreboard and Subscriber.

Verify the features like Burst transfer, aligned/non-aligned address, and pipelined operations.

1. **Verification of AMBA Protocol- APB Slave APB 3.0**

APB (Slave) with PREADY, PSLVERR – In-house Project

**Description:** APB is designed for low bandwidth control accesses, for example peripheral interfaces on system. This bus has an address and data phase but a much reduced, low complexity signal list. Furthermore, it is an interface designed for a low frequency system with a low bit width (32 bits).

**Roles and Responsibilities:**

AMBA-APB protocol specification.

Created Verification Plan.

Created Verification Environment using UVM Methodology.

Worked on Write & Read Sequence, Driver, Monitor, Scoreboard and Subscriber.

Performed read and write operations with and without wait states. Also, Slave Error Situation.

**Certification**

1. Organizer of TEQIP-III sponsored programme on ETODA'19
2. Online Certification Courses on System Verilog, UVM, Functional Coverage, Assertion, SOC Design.

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| **Education** |  |
| 2012 – 2016 | **B. Tech ECE** |
|  | Netaji Subhas University of Technology (East Campus),  formerly AIACTR |
|  | 74.81% |
| 2012 | **Intermediate | PCM with C++ | CBSE Board** |
|  | Jain Bharti Model School, Delhi |
|  | 82.6% |
| 2010 | **High School | CBSE Board** |
|  | Jain Bharti Model School, Delhi |

8.4 CGPA